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Design and development of PWM switching for 5-level multiphase interleaved DC/DC boost converter

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ABSTRACT

The continuously increasing demand for control on electric power equipment has led to the rapid technological development in various applications such as renewable energy, electric drives, and communication. Pulse Width Modulation (PWM) switching is an important technique to control the output voltage. PWM signals can either be generated using digital controller or analog controller. Digital controllers are widely used to generate PWM signals due to their reliability in solving complex algorithms within short amount of time. Multiphase boost converter is capable to overcome high input current ripple, current stress and semiconductor losses in conventional boost converter. This paper proposes a PWM switching scheme for multiphase interleaved converter using Field Programmable Gate Array (FPGA). The proposed switching scheme uses PWM switching technique that is implemented by programming Altera DE2-70 board. The duty cycle can be easily adjusted using assigned switches on the Altera board. For validation, switching frequency was set to 100 kHz, and then switching signal was observed using oscilloscope.

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1. INTRODUCTION

DC/DC converters are commonly applied in fields of renewable energy, automotive, and communication. There are types of DC/DC converters such as buck, boost, buck-boost, Sepic, Cuk and Flyback [1]. Conventional or single-phase DC/DC converters have certain limitations such as high current stress, high input current ripple, and less efficiency [2]. Another drawback is high conduction loss in the switching devices, which is a major constraint since it affects the output power of the converter [3].

One promising solution is by using DC/DC converters with multiphase configuration. It is basically a combination of conventional DC/DC converter in parallel arrangement. There are advantages of using multiphase configurations, such as reduction of current stress, high current output, low conduction loss, and high efficiency [4-8]. Besides, the size and rating of the components are reduced due to the split of input current into each circuit path. Basically, the performance of multiphase configurations depends on the PWM switching schemes. Multiphase DC/DC converter with interleaved switching technique is able to reduce input current ripple. Interleaved techniques means all power stages are operated in the phase, shifted to each other with the same frequency and duty cycle [9]. By using interleaving technique, the PWM switching signals in each phase can be operated in non-overlapped or overlapped conditions. When the multiphase is operated in non-overlapped conditions, minimum input current ripple can be achieved [10]. Nonetheless, the input

current ripple will still linearly increase as the switching signals are overlapped. Therefore, suitable duty cycle has to be considered in order to gain non-overlapped conditions. Thus, designation of PWM switching signals plays an important role in controlling the switches to solve those issues.

PWM switching is widely used in power converters, to emit signals to trigger the switch by turning on and turning off the switch [11]. Therefore, the current flowing through the switch can be controlled by manipulating the PWM switching signals. The PWM signals either can be generated using analog or digital controller. Analog circuit requires a large number of passive components, which is directly proportional to the complexity of the switching signals [12]. This is somewhat a limitation that reduces the system reliability and increases circuit complexity and space requirements. Thus, it is desirable to lessen complex mathematical operation due to the limitation in computational capability [13]. Moreover, analog system is hardly to configure without changing its hardware circuit [14].

Nowadays, digital circuits are more widely used compared to analog circuits. Digital systems can be operated in complex control strategies with powerful mathematical algorithms [15]. Moreover, complex control can be realized in short time by using supreme computational software. The most common digital controllers are Digital Signal Processing (DSP) and Field Programmable Gate Arrays (FPGA).

DSP commonly is used for solving complex mathematical algorithm with floating points operations, as in [16, 17]. This system operates in series, thus requires multiple DSP in order to operate for parallel circuit. PWM signals are less accurate when high switching frequency is applied. Compared to DSP controller, FPGA is more suitable for operation of high switching frequency due to the accuracy of its PWM signals. Besides, this controller is able to operate at the same time in the parallel circuit [18-20]. Thus, space areas can be reduced, as well as the cost of the controller.

This paper highlights the design and development of PWM switching signals for 5-level multiphase interleaved DC/DC converter. Initially, each switching signals range is clearly identified to avoid overlapping of signals. The switching signals are designed using Quartus II software. The signals are set at 60 degrees out of phase to each other. The duty cycle can be set by using assignment pins synchronizing to an internal counter.

2. PRINCIPLE OF 5-LEVEL MULTIPHASE CONVERTER OPERATION

In this paper, 5-level multiphase boost converter is proposed. This converter consists of five inductors, five switches and five diodes. Therefore, this converter requires five PWM signals to trigger each switch in the converter. Figure 1 shows the circuit configurations for 5-level multiphase boost converter.

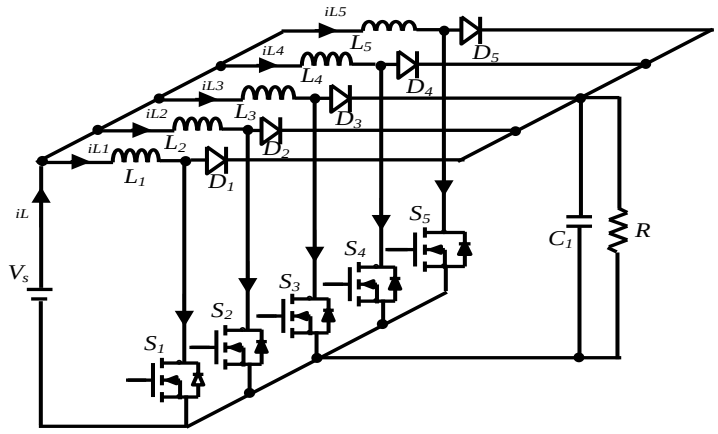


Figure 1. 5-level multiphase configurations

Meanwhile, Figure 2 shows the PWM switching signals for 5-level multiphase boost converter using interleaved technique. The switching signals are phased-shifted by 60 degrees to balance the charging and discharging of inductors over one period of time. Therefore, the inductor current in every phase cancels each other to reduce the input current ripple. The charging time of each inductor can be controlled by adjusting the duty cycle. The charging time of inductor is only increased once the duty cycle has increased. Thus, the output voltage also increases as the charging time of inductor is increased. The output voltage can be calculated by using (1);

$$V_{out} = \frac{V_{in}}{1-D} \tag{1}$$

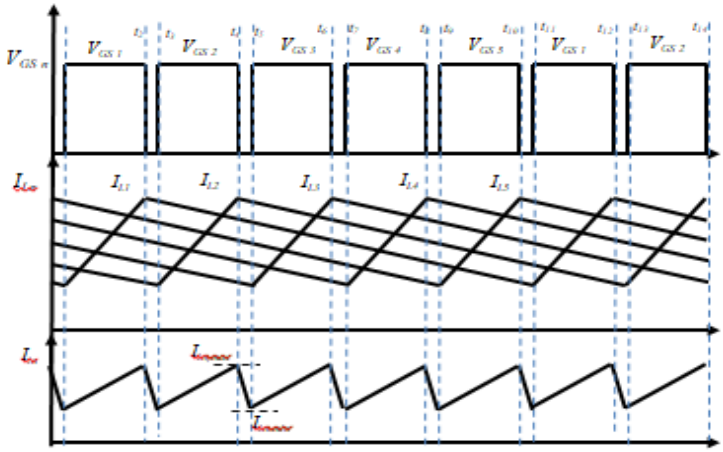


Figure 2. PWM switching signals for 5-level multiphase boost converter

In 5-level multiphase converter, there are 10 modes of operations for one cycle. Table 1 shows the modes operations for 5-level multiphase converter. During stages 1, 3, 5, 7, and 9, only one switch is turned-on, while the other switches are turned-off. Meanwhile, all switches are off during stages 2, 4, 6, 8 and 10.

Table 1. Circuit Parameter

Time	Switch, S_n	Diode, D_n
t_1-t_2 (Stage 1)	S_1 is ON while others are OFF.	D_1 is OFF while others are ON
t_2-t_3 (Stage 2)	All switches (S_1, S_2, S_3, S_4, S_5) are OFF.	All diodes (D_1, D_2, D_3, D_4, D_5) are ON.
t_3-t_4 (Stage 3)	S_2 is ON while others are OFF.	D_2 is off while others are ON
t_4-t_5 (Stage 4)	All switches (S_1, S_2, S_3, S_4, S_5) are OFF.	All diodes (D_1, D_2, D_3, D_4, D_5) are ON.
t_5-t_6 (Stage 5)	S_3 is ON while others are OFF.	D_3 is OFF while others are ON
t_6-t_7 (Stage 6)	All switches (S_1, S_2, S_3, S_4, S_5) are OFF.	All diodes (D_1, D_2, D_3, D_4, D_5) are ON.
t_7-t_8 (Stage 7)	S_4 is on while others are OFF.	D_4 is off while others are ON
t_8-t_9 (Stage 8)	All switches (S_1, S_2, S_3, S_4, S_5) are OFF.	All diodes (D_1, D_2, D_3, D_4, D_5) are ON.
t_9-t_{10} (Stage 9)	S_5 is ON while others are OFF	D_5 is OFF while others are ON
t_{10}-t_0 (Stage 10)	All switches (S_1, S_2, S_3, S_4, S_5) are OFF.	All diodes (D_1, D_2, D_3, D_4, D_5) are ON.

When the *n*-switch is ON, the inductor current on *n*-phase is charging while the others are discharging. The inductor current rate of change can be calculated using (2) and (3):

$$\text{Switch on} = \sum_{k}^{n} \frac{di_k}{dt} = \frac{V_s}{L_k} \tag{2}$$

$$\text{Switch off} \sum_{j}^{n} \frac{di_j}{dt} = \frac{V_s - V_0}{L_j} \tag{3}$$

where $j \neq k$
k is the ON switch and j is the OFF switch

The parameters of the multiphase converter are calculated by using equations in [21]. Some parameters such as input voltage and switching frequency are set to be fixed value in order to calculate the minimum parameters of inductor and capacitor. The minimum parameters of capacitor and inductor value are important to ensure that the converter operates in Continuous Current Mode (CCM) or Discontinuous Current Mode (DCM). In high power applications, CCM is more suitable compared to the DCM due to low input current ripple and low conduction losses. Besides, CCM generates non-pulsate current and the value of input current is not less than or equal to the zero values [22, 23]. Thus, the lifetime of the converter can greatly be improved. Table 2 shows the parameter for 5-level multiphase DC/DC boost converter.

Table 2. Circuit Parameters

Parameters	Value
Input voltage, V	15 V
Switching frequency, f_s	100 kHz
Inductor, L	220 µH
Capacitor, C	470 µF
Resistor, R	150 Ω

3. SIMULATION USING ORCAD PSPICE SOFTWARE

In this study, OrCAD PSpice software was used to simulate the parameters of the 5-level multiphase DC/DC boost converter before implementation into hardware prototypes. The parame-ters had been set in this software based on calculated parameters. Figure 3 shows the multiphase DC/DC boost converter model using OrCAD PSpice software.

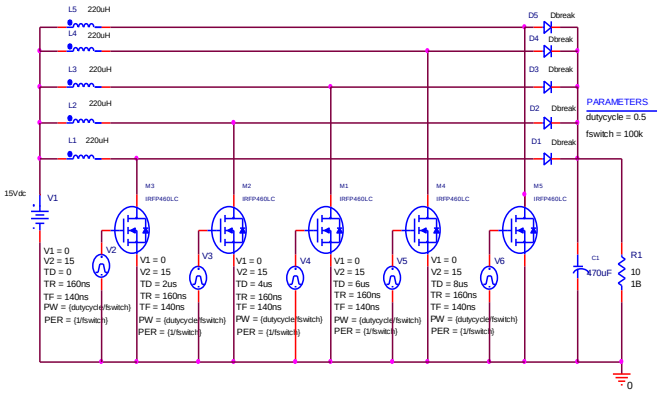


Figure 3. 5-level multiphase DC/DC boost converter model in OrCAD PSpice software

4. QUARTUS II SOFTWARE

Quartus II software was used to design the PWM switching signals. This software uses schematics or a hardware description language (HDL) such as Verilog HDL or VHDL. Figure 4 shows a flowchart representing the algorithm workflow of 5-level multi-phase boost converter.

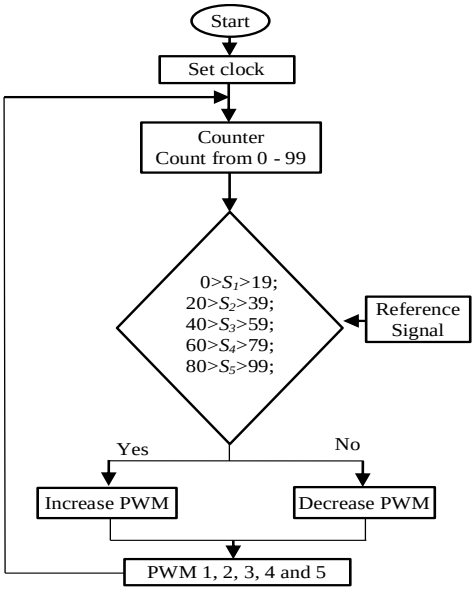


Figure 4. Flowchart of 5-level PWM signal

Initially, the clock is set by using *altpll* megafunction block diagram (.vhd). The *altpll* megafunction block is used to adjust the phase of generated signal to match the phase of an input signal. The input of *altpll* is connected with 50 MHz internal clock from *PIN_AD15* to generate a 10 MHz output. Then, the 10 MHz output frequency is connected to the *lpm_counter*. The function of *lpm_counter* is to generate binary counter which operates either in up, down or up/down counter. The counter is set to 7 bits with up-counter. Therefore, the counter will count from 0-99 for one complete cycle; representing 1ms period for one cycle for proffered frequency. Output from the *lpm_counter* will be sent to the comparator block to generate the PWM switching signals. The switching frequency of 100 kHz will be automatically set at the output of *lpm_counter*. In this study, since the output of *lpm_counter* was connected to each comparator, and five-phase multiphase boost converter being used, five comparators had been employed.

The comparators function to compare the input and the continuing *lpm_counter* in order to produce signal for S_1, S_2, S_3, S_4 and S_5. The conditions or ranges in each comparator are set by using IF ELSE statement in VHDL coding. The boundaries for each signal are set differently in order to phase-shift the output signals. The maximum on-state for each signal is 1/5 of the main clock. For example, the signal S_1 is only turned on from counter 0 to 19, while counter S_2 is from 20 to 39, counter S_3 is from 40 to 59, counter S_4 is from 60 to 79, and counter S_5 is from 80 to 99. Figure 5 shows the concept of 5-level interleaved signal using digital technique.

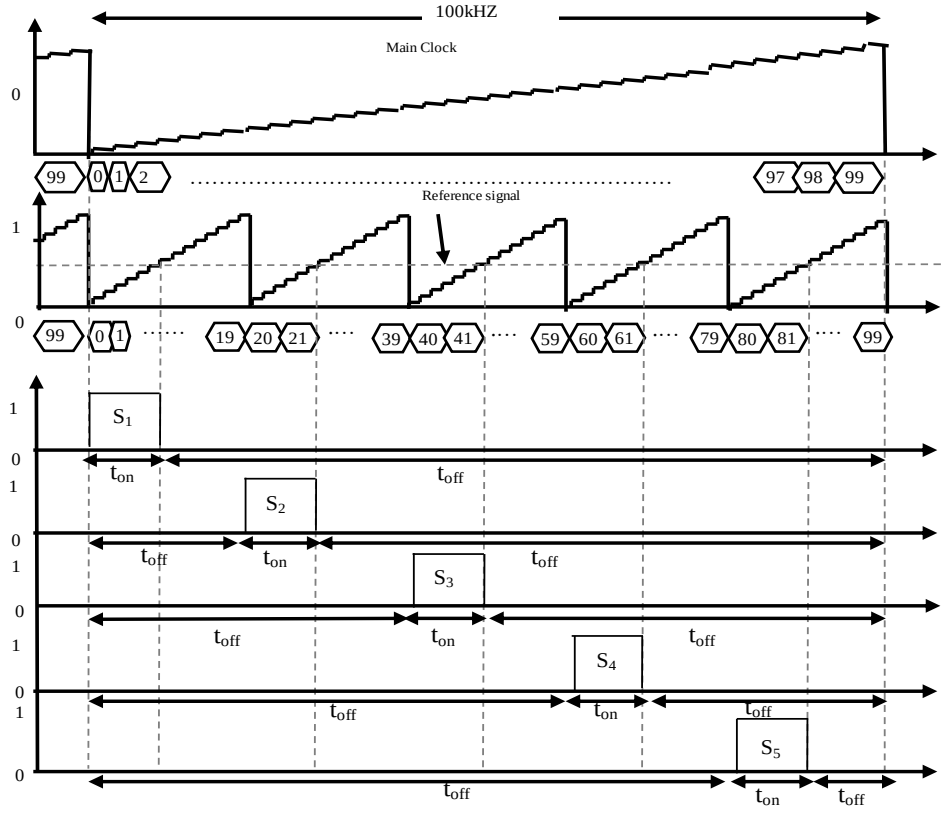


Figure 5. Associated PWM technique using digital implementation for 5-level interleaved signal

Once the compilation of the VHDL code is successful, the VHDL code will be converted into bdf schematic. The block diagram editor allows user to represent the whole system in single diagram. Figure 6 shows a PWM switching signals generator block diagram that has been programmed using Quartus II software. Series of pins are assigned such as input clock, slider switches and input/output. The slider switches are used to adjust the duty cycle.

In this study, the counter was set to 7-bit, therefore, 7 toggle switches had been assigned as the inputs in order to control the duty cycle in the converter. Table 3 shows the pin assignments for 5-phase PWM switching signals program. By referring to pin assignments, the location and direction of input and output connections can be determined. Table 4 shows the toggle switches for the 7-bit counters. Hence, the duty cycle can be manually adjusted by using assigned switches in FPGA board.

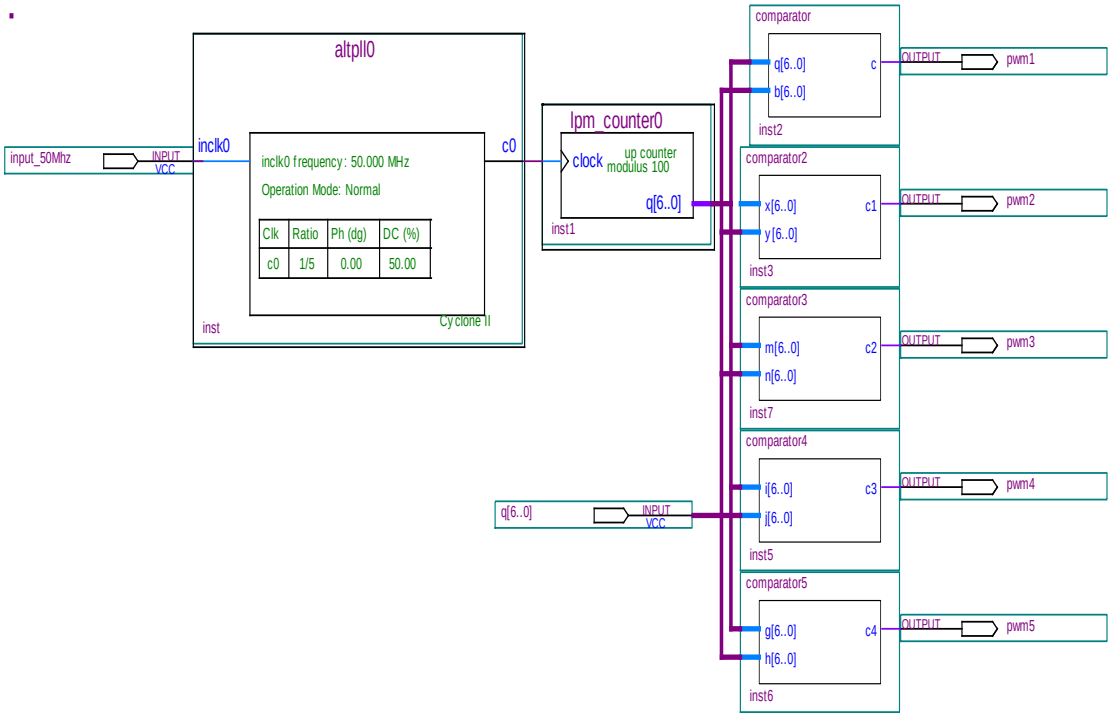


Figure 6. 5-level multiphase boost converter signals generator

Table 3. Pin Assignments for 5-phase PWM Switching Signals Program

Node name	Pin location	Description
Input_50MHz	PIN_AD15	50MHz FPGA internal clock
b[0]	PIN_AA23	Slider switch 0
b[1]	PIN_AB26	Slider switch 1
b[2]	PIN_AB25	Slider switch 2
b[3]	PIN_AC27	Slider switch 3
b[4]	PIN_AC26	Slider switch 4
b[5]	PIN_AC24	Slider switch 5
b[6]	PIN_AC23	Slider switch 6
pwm1	PIN_P30	General-purpose input/output (GPIO) connection [1]
pwm2	PIN_P29	General-purpose input/output (GPIO) connection [2]
pwm3	PIN_N29	General-purpose input/output (GPIO) connection [3]
pwm4	PIN_N28	General-purpose input/output (GPIO) connection [4]
pwm5	PIN_R27	General-purpose input/output (GPIO) connection [5]

Table 4. Toggle Switches For 7 bits Counters

Duty Cycle (%)	2^6 64	2^5 32	2^4 16	2^3 8	2^2 4	2^1 2	2^0 1	Decimal
10	0	0	0	1	0	1	0	10
20	0	0	1	0	1	0	0	20
30	0	0	1	1	1	1	0	30
40	0	1	0	1	0	0	0	40
50	0	1	1	0	0	1	0	50
60	0	1	1	1	1	0	0	60
70	1	0	0	0	1	1	0	70
80	1	0	1	0	0	0	0	80
90	1	0	1	1	0	1	0	90
100	1	1	0	0	1	0	0	100

In interleaved techniques, the dead-time or blanking time should be considered in order to reduce current spike across the switch during turning-on and turning-off of each switch. Dead-time is a time delay,

which allows inverting switching signals into turn-off before the other turn-on. In this study, Metal Oxide Semiconductor Field Effect Transistor (MOSFET) was used as the power switch. This type of switch has a gate for charge and discharge time rather than instantly turning on and off. Without dead-time, the PWM switching signals will overlap each other, which means two switches will be turned on for a small period of time. The function of dead-time is to avoid unnecessary heating and high losses to the converter [24-26].

Dead-time is added by reducing the counter division in each comparator. By doing this, the signal's duty cycle will be compromised. For example, when the duty cycle is set at 0.2, the signal duty cycle should appear at 0.18 when observed using oscilloscope; however, when the fall time and rise time are considered, the signal actually takes the capacity of 0.2 duty cycle.

5. RESULT AND ANALYSIS

The output of the Altera DE2-70 was observed using Tektronix TDS2014B four channel oscilloscope. Since the oscilloscope can only read maximum four waveforms, only four waveforms were obtained for five-phase PWM signals.

In Figure 7, CH1 represents the first PWM signal, CH2 represents the second PWM signal, CH3 represents the third PWM signal, and CH4 represents the fourth PWM signal. From the waveforms captured by Tektronix TDS2014B, it can be observed that all the PWM signals had been turned on in interleaving manner with the switching frequency of 100 kHz. The voltage for PWM signals from Altera DE2-70 board was 3.33 V.

The gate driver was used to boost the voltage magnitude of the signals from 3.33 V to 15 V to make sure that the signals able to trigger the MOSFET. The gate and source pin of the MOSFET were connected to the output of the gate driver for control, so that the PWM signals would control the ON and OFF period of the MOSFET with the reference duty cycle. Figure 8 shows the PWM signals output from the gate driver.

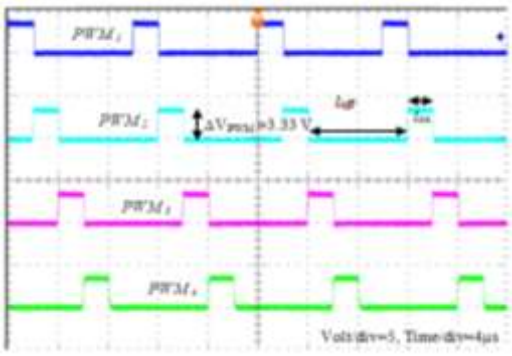


Figure 7. PWM signals output from Altera

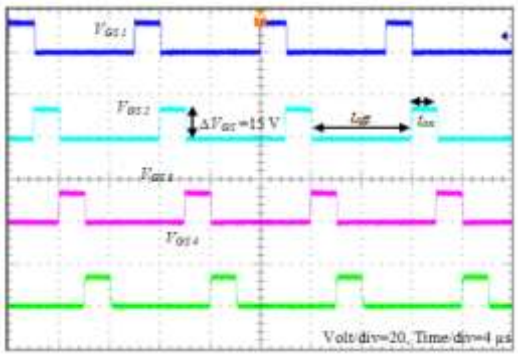
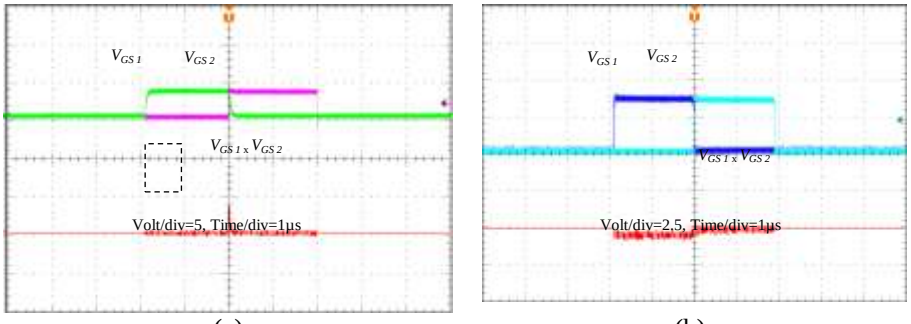


Figure 8. PWM signal output from gate driver

Figure 9 shows the PWM signals without dead-time and with dead-time. As shown in Figure 9(a), the crossover between PWM 1 and PWM 2 caused spike to the signals. Meanwhile, no spike was occur when dead time is implements, as shown in Figure 9(b).



(a) (b)

Figure 9. PWM signals (a) without dead-time and (b) with dead-time

Table 5. Output Voltage in Simulation and Experimental

Duty Cycle, D	Output Voltage, V_o	
	Simulation (V)	Experimental (V)
0.05	17.29	16.20
0.10	18.72	17.60
0.15	20.66	18.90
0.20	22.73	20.80

The experimental setup for 5-level multiphase boost converter are carried by using Altera DE2-70 as a microcontroller. From the results in Table 5, it can be seen that the values of the output voltage produced by experiment and simulation slightly differ, which might be due to factors such as switching losses, conduction losses and number of phase. The inserted dead-time also significantly changed the behavior of the actual duty cycle, causing a small voltage drop compared to simulation. Nonetheless, the results show that the multiphase converter can work correctly theoretically; indicating that the proposed design can be implemented as part of multiphase converter, in addition to power circuit using PWM as its control scheme.

6. CONCLUSION

This paper has presented a specifically designed PWM switching signals to meet the needs of the multiphase DC/DC boost converters. The PWM switching signals are generated by using VHDL programming in FPGA controller. Other programming languages such as Verilog, C languages and logic form are applicable with the FPGA controller. By using interleaved technique, the PWM switching signals are set to phase-shift in each level. This technique can be realized by setting the reference signals in every comparator. Comparison between the simulation and experimental results shows a small difference in output voltage.

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